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10/647,805	08/25/2003	Ira Liao	3304.2.81	2355

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EXAMINER
CHAUHAN, ULKA J

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/647,805	LIAO ET AL.
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL.** 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-21_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-21_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _25 August 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _10/18/04_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Priority

1.   Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers

have been placed of record in the file.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.   **Claims 1-4, 16, 17, 20, and 21 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over U.S. Patent No. 5,943,064 to Hong and U.S. Patent No. 6,621,499 to

Callway.

5.   As per claim 1, Hong teaches a computer graphics system comprising:

image pickup device (Fig. 2 and c. 5 ll. 32-34: *The video capture port is used to receive digital*

video pixel data for digital processing, storage, and display);

an image data storage unit (Fig. 2 and c. 5 ll. 26-28: *frame buffer 18 has a graphics buffer*

segment 20 for storing graphics data and a video buffer segment 22 for storing video

data) in communication with said compressing device and said system memory (Fig. 2:

system memory 34) for storing said compressed image data (c. 5 ll. 55-67: *video pixel*

data is stored in a compressed format to use less memory); and

a data decompressing device in communication with said image data storage unit and said image

displaying device, decompressing said compressed image data stored in said image data

storage unit to recover said digital image data that is then transmitted to said image

displaying device for display (c. 6 ll. 1-4: *the video display engine 26 decompresses the*

compressed video pixel data before the resulting video pixel data is transmitted to the

display device).

6.   Hong disclose that the video source generates a signal under the MPEG compression

standard (c. 5 ll. 42-44) and that compressed video data is stored in the video segment of the

frame buffer (c. 5 ll. 56-67), but fails to expressly teach a data compressing device compressing a

digital image data received from said image pickup device into a compressed image data.

Callway, in the same field of endeavor as Hong, teaches a video processing device comprising a

video graphics controller connected through a common port to an MPEG video decompressor

and an MPEG video compressor used to convert data to and from the graphics controller to

suitable compressed or decompressed format (c. 2 ll. 14-28). It would have been obvious to one

of ordinary skill in the art at the time the invention was made to have utilized an MPEG

compressor as taught by Callway in combination with Hong's computer graphics system in order

compress the captured digital video data thereby reducing the amount of memory space required

for storing the same.

7.   Hong also does not expressly teach transmitting the compressed image data to the system

memory in a DMA mode. Callway discloses that the MPEG compressor 66 compresses data

being transmitted to the host (Figs. 1, 4, and 5). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to have utilized transmitting compressed data

to the host as taught by Callway in combination with Hong's computer graphics system in order

to store the compressed data in the host's system memory for further processing or storage. One

would have been motivated to transmit the data in a DMA mode in order to transfer the data

more quickly without requiring any intervention by the CPU.

8.   As per claim 2, Hong discloses that the data decompressing device is integrated into a

graphics chip (Fig. 2: *graphics controller chip 15 comprising the video display engine 26 that*

decompresses the compressed video pixel data). Hong does not expressly teach that the data

compressing device is integrated into a graphics chip. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to have integrated an MPEG

compressor into Hong's graphics controller chip in order to reduce system cost while increasing

system performance through integration.

9.   As per claim 3, Hong discloses that the graphics chip is disposed in a graphics card (Fig.

2: *graphics card 13 comprising graphics chips 15 and 32*).

10.   As per claim 4, Hong discloses that the image data storage unit is a frame buffer defined

in a local memory of said graphics card (Fig. 2: *graphics card 13 comprising a frame buffer 18*).

11.   Claims 16, 17, 20, and 21 are similar in scope to claims 1 and 3, and are rejected under the same rationale.

12.   Claims 5, 7, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong and U.S. Patent No. 6,621,499 to Callway and Applicants' Admitted Prior Art (APA) [0002-0004].

13.   As per claim 5, Hong teaches a computer graphics system comprising:

image pickup device (Fig. 2 and c. 5 ll. 32-34: *The video capture port is used to receive digital video pixel data for digital processing, storage, and display*);

an image data storage unit (Fig. 2 and c. 5 ll. 26-28: *frame buffer 18 has a graphics buffer segment 20 for storing graphics data and a video buffer segment 22 for storing video data*) in communication with said compressing device for storing said compressed image data (c. 5 ll. 55-67: *video pixel data is stored in a compressed format to use less memory*); and

a data decompressing device in communication with said image data storage unit and said image displaying device, decompressing said compressed image data stored in said image data storage unit to recover said digital image data that is then transmitted to said image displaying device for display (c. 6 ll. 1-4: *the video display engine 26 decompresses the compressed video pixel data before the resulting video pixel data is transmitted to the display device*).

14.   Hong disclose that the video source generates a signal under the MPEG compression standard (c. 5 ll. 42-44) and that compressed video data is stored in the video segment of the frame buffer (c. 5 ll. 56-67), but fails to expressly teach a data compressing device compressing a

digital image data received from said image pickup device into a compressed image data.

Callway, in the same field of endeavor as Hong, teaches a video processing device comprising a

video graphics controller connected through a common port to an MPEG video decompressor

and an MPEG video compressor used to convert data to and from the graphics controller to

suitable compressed or decompressed format (c. 2 ll. 14-28). It would have been obvious to one

of ordinary skill in the art at the time the invention was made to have utilized an MPEG

compressor as taught by Callway in combination with Hong's computer graphics system in order

compress the captured digital video data thereby reducing the amount of memory space required

for storing the same.

15.   Hong does not expressly teach that the image data storage device in disposed in the

system memory. APA discloses a conventional computer system (Fig. 1) for processing analog

signals from the TV tuner 15 and writing them in the frame buffer or in the AGP memory 131 of

the system memory 13 in a direct memory access (DMA) mode for further storage in a non-

volatile memory [0003]. It would have been obvious to one of ordinary skill in the art at the time

the invention was made to have utilized the AGP memory of the system memory as taught by

APA in combination with Hong's computer graphics system, whereby compressed digital video

data is stored in the AGP memory of the system memory in order to convert it into a file for

storage in a non-volatile memory device.

16.   As per claim 7, APA discloses AGP memory defined in the system memory (Fig. 1 and

[0003]).

17.   Claim 19 is similar in scope to claim 5, and is rejected under the same rationale.

18.   **Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong, U.S. Patent No. 6,621,499 to Callway, Applicants' Admitted Prior Art (APA) [0002-0004], and U.S. Patent No. 6,630,936 to Langendorf.**

19.   As per claim 6, Hong discloses that the data decompressing device is integrated into a graphics chip (Fig. 2: *graphics controller chip 15 comprising the video display engine 26 that decompresses the compressed video pixel data*). Hong does not expressly teach that the data decompressing and data compressing devices are integrated into a graphics chip disposed in a north-bridge chip. Langendorf teaches a computer graphics system in which the graphics controller is integrated into a single graphics and memory controller hub that delivers high performance 3D, 2D, and motion compensation video capabilities, and that is implemented as a PCI chip or a host chip set (Fig. 4 and c. 3 ll. 48-c. 4 ll. 19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the integrated PCI or host chip set taught by Langendorf in combination with Hong's computer graphics system whereby the MPEG compressor taught by Callway along with the decompressor taught by Hong are integrated into a PCI or host chip set taught by Langendorf in order to increase performance as a result of integration, while reducing system costs.

20.   Claim 18 is similar in scope to claim 6, and is rejected under the same rationale.

21.   **Claims 8-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong, U.S. Patent No. 6,621,499 to Callway, and U.S. Patent No. 6,630,936 to Langendorf.**

22.   As per claim 8, Hong discloses a computer graphics system comprising:

a system memory accessible by said core logic unit (Fig. 2: *system memory 34*);

an image pickup device receiving and converting an analog image signal into a digital image

    data (Fig. 2 and c. 5 ll. 32-34: *The video capture port may also receive analog video*

    signals, which it may convert to digital video pixel data);

an image data storage unit (Fig. 2 and c. 5 ll. 26-28: *frame buffer 18 has a graphics buffer*

    segment 20 for storing graphics data and a video buffer segment 22 for storing video

    data) for storing therein said compressed image data;

a data decompressing device in communication with said image data storage unit, decompressing

    said compressed image data stored in said image data storage unit to recover said digital

    image data; and an image display device in communication with said data

    decompressing device, receiving and displaying said digital image data (c. 5 ll. 55-67:

    video pixel data is stored in a compressed format to use less memory).

23.   Hong disclose that the video source generates a signal under the MPEG compression

standard (c. 5 ll. 42-44) and that compressed video data is stored in the video segment of the

frame buffer (c. 5 ll. 56-67), but fails to expressly teach a data compressing device compressing a

digital image data received from said image pickup device into a compressed image data.

Callway, in the same field of endeavor as Hong, teaches a video processing device comprising a

video graphics controller connected through a common port to an MPEG video decompressor

and an MPEG video compressor used to convert data to and from the graphics controller to

suitable compressed or decompressed format (c. 2 ll. 14-28). It would have been obvious to one

of ordinary skill in the art at the time the invention was made to have utilized an MPEG

compressor as taught by Callway in combination with Hong's computer graphics system in order

compress the captured digital video data thereby reducing the amount of memory space required for storing the same.

24.   Hong discloses a memory controller 10 (Fig. 1) but does not expressly teach a core logic unit. Langendorf teaches a computer graphics system in which the graphics controller is integrated into a single graphics and memory controller hub that delivers high performance 3D, 2D, and motion compensation video capabilities, and that is implemented as a PCI chip or a host chip set (Fig. 4 and c. 3 ll. 48-c. 4 ll. 19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the integrated PCI or host chip set taught by Langendorf in combination with Hong's computer graphics system so that communication amongst the CPU, system memory, graphics controller, and PCI bus can be easily and efficiently managed.

25.   As per claim 9, Hong discloses that the data decompressing device is integrated into a graphics chip (Fig. 2: *graphics controller chip 15 comprising the video display engine 26 that decompresses the compressed video pixel data*). Hong does not expressly teach that the data compressing device is integrated into a graphics chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated an MPEG compressor into Hong's graphics controller chip in order to reduce system cost while increasing system performance as a result of integration.

26.   As per claim 10, Hong discloses that the graphics chip is disposed in a graphics card in communication with said core logic unit (Fig. 2: *graphics card 13*).

27.   As per claim 11, Hong discloses that the image data storage unit is a frame buffer defined in a local memory of said graphics card (Fig. 2: *frame buffer 18*).

28.   As per claim 12, Langendorf discloses that the graphics chip is integrated with said core logic unit (Fig. 4: *graphics and memory controller hub 210 including graphics controller 212*).

29.   As per claim 13, Langendorf discloses that the core logic unit is a north-bridge chip (Fig. 4: *graphics and memory controller hub 210 within chipset 200*).

30.   As per claim 15, Hong discloses that the image pickup device and said image display device are disposed in a graphics card (Fig. 2: *video capture port 30 and display engines 24 and 26*).

31.   **Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong, U.S. Patent No. 6,621,499 to Callway, U.S. Patent No. 6,630,936 to Langendorf, and Applicants' Admitted Prior Art (APA) [0002-0004].**

32.   As per claim 14, Hong does not expressly teach that the image data storage unit is a specified memory block defined in said system memory. APA discloses a conventional computer system (Fig. 1) for processing analog signals from the TV tuner 15 and writing them in the frame buffer or in the AGP memory 131 of the system memory 13 in a direct memory access (DMA) mode for further storage in a non-volatile memory [0003]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the AGP memory of the system memory as taught by APA in combination with Hong's computer graphics system, whereby compressed digital video data is stored in the AGP memory of the system memory in order to convert it into a file for storage in a non-volatile memory device.

Conclusion

33.   The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20030234749A1   US 20030016226A1   US006717987B1   US006557065B1

     US005990958A   US005812789A

34.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The

examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

35.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

36.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 14, 2005